APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY **A**

Second Semester M.Tech. Degree Examination, MAY-2017.

COMPUTER SCIENCE & ENGINEERING

(Computer Science & Engineering)

01CS6102: PARALLEL COMPUTER ARCHITECTURE

Time : 3 Hrs. Max. Marks : 60

(Answer any 2 questions from each Part)

Part A

(Modules - I & II)

1. (a) Determine the number of clock cycles required to process a program with 300 instructions in a five segment pipeline. [2]

   (b) Find the CPU needed for executing 80K program with a processor of speed 100 MIPS. [3]

   (c) Explain the concept of forwarding mechanism used in pipelining. [4]

2. (a) Derive an expression for overall speedup according to Amdahl's Law. [4]

   (b) When a computation is run in vector mode on the vector hardware, it is 20 times faster than the normal mode of execution. We call the percentage of time that could be spent using vector mode the *percentage of vectorization*. What percentage of vectorization is needed to achieve a speed up of 3 ? [3]

   (b) What do you understand by control hazards. [2]

3. (a) A processor of speed 2 GHz is used to execute a program with the following details:

Arithmetic instructions		50K	1 (CPI)
Memory	"	20K	2 "
Control	"	10K	2 "
I/O	"	10K	3 "

   Find the CPU time needed for the execution of the program. [3]

   (b) What do you understand by pipeline scheduling. [2]

   (c) Write the dependencies existing between the various instructions in the following code

DIV.D	F0, F2, F4
ADD.D	F6, F0, F8
S.D	F6. 0(R1)
SUB.D	F8, F10, F14
MUL.D	F14, F1,F10

[4]

Part B

(Modules - III & IV)

4. (a) What is the purpose of Reservation stations in a machine that uses Tomasulo's scheme, also write its structure. [5]

   (b) How strides can be used for handling multidimensional arrays in vector architecture. [4]

5. (a) Explain the different steps involved in hardware based speculation. [4]
   (b) Whether this loop can be vectorized in normal case? Justify your answer.

```
for (i=0; i<32;  i++)
        if ( X[i] != 0 )
                X[i] = X[i] – Y[i]
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   If possible explain how vector mask register can be used to vectorize this. [5]

6. (a) Explain about the two different approaches used to issue multiple instructions per clock in a dynamically scheduled processor. [4]
   (b) Compare C-Access and S-Access vector-access memory schemes with figures. [5]

Part C
(Module – V & VI)

7. (a) Compare Centralized shared memory architecture and Distributed shared memory architecture. [6]
   (b) Explain the concept of a directory-based cache coherence scheme. [6]

8. (a) How an 8 x 8 Omega network can be built with 2 x 2 switches for the permutation (1,7,4,5,2)(0,3)(6). Explain the routing of a message from input 100 to output 101. [6]
   (b) What is multiprocessor cache coherence? Explain the reasons which cause cache inconsistencies. [6]

9. (a) Explain about hierarchical bus system. [3]
   (b) What do you understand by multiport memory. [3]
   (b) Draw the state transition diagram of a write invalidate cache coherence protocol for a private write back cache. Explain about different states and state transitions. [6]

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