

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.Tech DEGREE EXAMINATION DECEMBER 2015

**D**

ELECTRONICS AND COMMUNICATION ENGINEERING

Signal Processing

01EC6307 DSP SYSTEM DESIGN

Time 3 Hours

Max.Marks:60

*Answer any two questions from each module*

**MODULE I & MODULE II**

1. a) Give the basic computational blocks of a DSP Processor. (4)  
b) Explain with example IEEE 754 Single and double precision floating point representation format. (5)
2. a) Given an RNS system (32/31/15/7) .  
Represent the number  $x=168$  &  $y=-23$  in this RNS  
Compute  $x+y$  ,  $x-y$  ,  $x*y$ . (5)  
b) What is the limitation of Distributed Arithmetic? (4)
3. Compute Sin 30 & Cos 30 to a precision of 5 bits by CORDIC Algorithm. (9)

**MODULE III & MODULE IV**

4. What is pipelining? Explain the performance issues in pipelining. (9)
  5. Show how the following code would look on MIPS. Compute the clock cycles required per element processing. (9)
    - i) Unscheduled
    - ii) scheduled
    - iii) loop-unrolled but unscheduled and
    - iv) loop-unrolled and scheduled including any stalls or idle clock cycles, ignoring delayed branches.
- ```
LOOP:  L.D      F0, 0(R1);  
        ADD.D   F4,F0,F2  
        S.D     F4,0(R1)  
        DADDUI  R1,R1#-8  
        BNE     R1,R2,LOOP
```
6. a) With a diagram, explain Tomasulo's algorithm for Dynamic Scheduling. (5)  
b) Differentiate hazard and dependency (4)

## MODULE V & MODULE VI

7. a) Assume a computer where the CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer if all instructions were cache hits? (6)
- b) Give any three optimization techniques to improve cache performance (6)
8. a) Explain the limitations of ILP . (6)
- b) Explain the features of code composer studio of TMS 320C 6713 Processor (6)
9. a) Explain the memory architecture of TMS 320C 6713 Processor. (6)
- b) Write an assembly language program to implement  $\sum_{n=1}^{10} a(n).x(n)$  (6)

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