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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2017

Electronics & Communication Engineering

Signal Processing

01EC6307 DSP System Design.

Answer *any two full* questions from *each* part

Limit answers to the required points.

Max. Marks: 60 Duration: 3 hours

PART A

1. a. Give the method to reduce the size of ROM by offset coding in Distributed Arithmetic. (4)

   b. Consider the RNS (8/7/5/3) (5)

      i) Represent the numbers x= 128 and y= 35 in this RNS
      ii) Convert (3/2/4/2) into decimal
      iii) Compute x+y, x-y

2. a. Consider a prime moduli p=17 , generator g=3 will generate the elements of a finite field. Compute a x b and a + b in index domain (a = 3 , b = 2) (4)

   Encoding table is given below.

a	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
$\text{ind}_3(a)$	$-\infty$	0	14	1	12	5	15	11	10	2	3	7	13	4	9	6	8

n	$-\infty$	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$Z(n)$	0	14	12	3	7	9	15	8	13	$-\infty$	6	2	10	5	4	1	11

   b. Give the basic features that must be provided in DSP architecture to implement convolution operation. (5)

3. a. Derive the equations required for the implementation of CORDIC algorithm. (6)

   Using this, compute sin (60) and cos (60) to a precision of 4 bits.

b. How can the 9 bit LNS coding 000111.0010 (radix 2, 2 sign bits, 3 bits for integer precision, 4 bit fractional precision)be translated into real number system ? (3)

PART B

4. a. Mention the performance issues in pipelining. Give the performance of pipeline with stalls. (4)

b. Explain how RAW hazards are resolved in the basic Tomasulo's algorithm. (5)

5. a. Draw the datapath for handling conditional branching instructions in MIPS. Also explain the various steps in the execution of a conditional branching instruction in a 5 stage pipelined processor. (5)

b. Identify all data dependencies in the following code, assuming that we are using the 5-stage MIPS pipelined datapath. Which dependencies can be resolved via forwarding? (4)


```
ADD R2,R5,R4
ADD R4,R2,R5
SW R5,100(R2)
ADD R3,R2,R4
```

6. a. With an example explain load use data hazard. How it can be eliminated? (4)

b. Differentiate hazard and dependency (2)

Identify the type of data hazards (3)

i)
```
add $s1, $s2, $s3
mul $s0, $s1, $t1
```

ii)
```
lw $s1,0($s2)
add $s2,$t1,$t0
```

iii)
```
sw $s1,0($t0)
add $s1,$s0,$t1
```


PART C

7. a. Give the limitations of Instruction level parallelism. (2)

b. With proper examples, explain the difference between linear and circular addressing modes in C 6713 processor. Specify the applications in which these addressing modes are used. (5)

c. Explain the various dynamic branch prediction schemes. (5)

8. a. Assuming a cache of 4K blocks, a two word block size and a 32 bit address, find total number of sets and total number of tag bits for cache that are direct mapped, 2 way , 4 way set associative and fully associative. (6)

b. Briefly explain the features of a TMS 320C6713 processor. (6)

9. a. Which has lower miss rate: a 16KB instruction cache with a 16KB data cache or a 32KB unified cache? (Assume 36% of the instructions are data transfer instructions, A hit takes 1 clock cycle and miss penalty is 100 clock cycles)A load or store hit takes 1 extra clock cycle on a unified cache if there is only 1 cache port to satisfy 2 simultaneous requests. What is the average access time in each case? Assume write through cache with a write buffer and ignore stalls due to write buffer. Misses/1000 instructions for instruction, data & unified cache of different size are given below. The percentage of instruction references is about 74 %. (6)

Size	Instruction Cache	Data Cache	Unified cache
16KB	3.82	40.9	51.0
32 KB	1.36	38.4	43.3

b. Write an assembly language program to implement $y(n) = x(n) * h(n)$ (6)