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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.TECH DEGREE EXAMINATION, DECEMBER 2017

Electronics & Communication Engineering

Signal Processing

01EC6307 DSP System Design.

Answer *any two full* questions from *each* part

Limit answers to the required points.

Max. Marks: 60 Duration: 3 hours

PART A

1. a. What is Residue number system? Give the conversion of (5/3/2/1) to decimal w.r.to RNS (8/7/5/3) (4)

   b. Show the multiplier adder graph for realizing the constant number 155 using signed digit number and factorization. (5)

2. a. Represent $(-0.5)_{10}$ in IEEE 754 single precision and double precision format. (4)

   b. Using the concept of carry free SD addition , compute 7+(- 4) (5)

3. a. Give the significance of shifter in a DSP system. (3)

   b. Compare Rotation mode and Vectoring mode. (6)

   Compute sin(30) and cos (30) to a precision of 4 bits using CORDIC algorithm.

PART B

4. a. Identify the type of hazard that exists in the MIPS code fragments given. (4)

   i) LD R1, 10(R2)
   ADD R3, R1,R2

   ii)DADD R1,R2,R3
   SD 100(R1),R4

   b. With a diagram, explain the basic pipeline stages in a 5 stage MIPS processor for handling a memory reference instruction. (5)

5. a. How data hazards can be eliminated using Tomosaulo's approach? (6)

   b. Briefly explain the instruction formats in MIPS. (3)

6. a. How are control hazards handled in pipelined processors? (5)

   b. Compare name dependency and data dependency. (4)

PART C

7. a. How many total bits are required for a DM cache with 16 KB of data and 4 word blocks, assuming a 32 bit address ? (6)

   b. What are the steps involved in handling an instruction in a processor with a branch target buffer? (6)

8. a. Assume we have a system where all the CPI is 1.0 when all memory accesses hit the cache. The only data access are loads and stores and these total 50 % of the instructions. If the miss penalty is 25 clock cycles and miss rate is 2 %, how much faster would the computer be if all the instructions were cache hits? (6)

   b. Explain the type of instructions in a TMS 320C6X processor. Also write an assembly language program to implement $y = \Sigma\, a(n) \,.\, x\,(n)$ [where $n = 0 : 9$] (6)

9. a. Give the optimization techniques to improve cache performance. (6)

   b. Briefly explain the memory architecture of TMS 320C6713 processor. (6)