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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SECOND SEMESTER M.TECH DEGREE EXAMINATION, APRIL 2017

Electronics and Communication

01EC6122 **Design of VLSI Systems**

Max. Marks : 60 Duration: 3 Hours

Part A (Answer any TWO Questions)

1) a) Draw the transfer characteristics of a static CMOS inverter and identify the different regions of the transfer characteristics as the V_{in} is swept from 0 to V_{DD} depending on the operating conditions of PMOS and NMOS transistors.

b) Define Noise margin in terms of neat figures. (4.5 X 2=9 marks)

2)(a) Explain the structure and working of pseudo-NMOS logic gate.

(b) Consider a CMOS process with V_{DD}=5V, V_{Tn}=+0.7 V, V_{Tp}=-0.8V, k_n=150μA/V^2 and k_p=68μA/V^2.Calculate V_{OL} for $(W/L)_n$=4 and

$(W/L)_p$=6. (4.5 X 2=9 marks)

3) a) Explain various issues of dynamic CMOS logic.Write down the solutions to overcome these drawbacks.

b)Explain the effect of capacitances in the dynamic behavior of CMOS inverter.

(4.5 X 2=9 marks)

Part B (Answer any TWO Questions)

4)Do the comparison study on propagation delay of square root carry- select adder versus linear ripple and select adders with the help of equations and supporting figures.

(9 marks)

5)With the help of necessary equations , explain how the switching activity affects power consumption of CMOS devices. Also explain different techniques to reduce the switching activity of CMOS devices.

(9 marks)

6) a) Compare the performance of Array multiplier with Carry- Save multiplier using

necessary diagrams.

b)Explain in detail about any one power reduction techniques done while designing a CMOS circuit

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(4.5 X 2=9 marks)

Part C (Answer any TWO Questions)

7)a) Explain the working of 4x4 MOS NAND ROM.

b) Explain the working of flash memory with transistor level circuit duiagram.

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(6 X 2=12 marks)

8)Compare the structure and working of Dynamic 2 to 4 NOR and NANDDecoders.

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(12 marks)

9) a)Describe the operation of 3T dynamic memory cell using timing diagram.

b)Briefly explain the working of basic differential sense amplifier circuit.

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(6 X 2=12 marks)
