

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**

**SECOND SEMESTER M.TECH DEGREE EXAMINATION, MAY 2016**

**Electronics & Communication**

**01EC6122 Design of VLSI Systems**

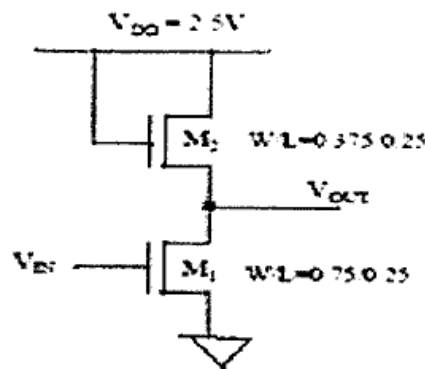
Max. Marks : 60

Duration: 3 Hours

**Instruction:** Answer any two questions from each module.

**PART A**

1. Calculate  $V_{OH}$ ,  $V_{OL}$  and  $V_{th}$  for the circuit.



(9 marks)

2. a) Obtain the CMOS implementation of a 6 input OR gate. (9 marks)
- b) Compute worst case propagation delay using Elmore delay model. (9 marks)
3. a) Explain why nMOS is used as a PDN and pMOS as PUN. (4 1/2 marks)
- b) Discuss the issues of dynamic logic. (4 1/2 marks)

**PART B**

4. Obtain the implementation of Wallace tree multiplier for 4x4 bit multiplication. Compare it with Dadda multiplier. (9 marks)
5. Discuss on scaling and power consumption (9 marks)
6. a) Explain how pipelining reduces power consumption (4 1/2 marks)
- b) For a ripple carry adder of bits  $A_k$  and  $B_k$  for  $k=0,1,2,3$ , obtain the worst case condition and delay. (4 1/2 marks)

**PART C**

7. a) Explain differential sensing. (6 marks)
- b) How differential sensing can be done for single ended output. (6 marks)
8. Discuss on various MOS memories. (12 marks)
9. a) Compare NAND ROM and NOR ROM. (6 Marks)
- b) Briefly explain CAM. (6 Marks)